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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,673	09/15/2003	Indrajit Manna	CS02-084	1857

7590 05/05/2005

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,673	MANNA ET AL.	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Election filed on 4/14/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *6-13,17 and 21-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,14,16 and 20* is/are rejected.

7)☒ Claim(s) *2,3,15,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 6-13, 17, and 21-27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 4/14/05.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 5, 14, 16, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,492,208 Cheng et al.

2. Referring to claim 1, an ESD protection device with complementary dual drain implant comprising: a) an N-well, (Figure 6 #612), implanted in a P-substrate, (Figure 6 #21); b) an N+ diffusion, (Figure 6 #624 & 620), implanted on top of said N-well, (Figure 6 #612), such that said N+ diffusion, (Figure 6 #624 & 620), extends into said P-substrate, (Figure 6 #21), on both

sides of said N-well, (Figure 6 #612); c) where said N+ diffusion, (Figure 6 #624 & 620), is shared by the drains of two adjacent NMOS transistors, (Figure 6 #626 & 618); d) a pad, (Figure 6 #38), coupled conductively to said N+ diffusion, (Figure 6 #624 & 620), between said drains; and e) a P-ESD implant, (Figure 6 #622), interposed between said N+ diffusion, (Figure 6 #624 & 620), and said N-well, (Figure 6 #612), such that said N-well, (Figure 6 #612), is electrically coupled to said N+ diffusion, (Figure 6 #624 & 620), where said P-ESD, (Figure 6 #622), implant lowers the avalanche voltage of a transistor by reducing the breakdown voltage, (All of the elements of the device as claimed are present in the referenced Figure 6, hence the device would function the same as claimed and Col. 4 Lines 50-60), of the drain/p-substrate junction, (Figure 6 #21).

3. Referring to claim 4, an ESD protection device, wherein said drains, (Figure 6 #624 & 620), of said two NMOS transistors, (Figure 6 #626 & 618), are at opposite ends of said N-well, (Figure 6 #612).

4. Referring to claim 5, an ESD protection device, wherein said N-well, (Figure 6 #612), extends in depth beyond the bottom of said P-ESD implant, (Figure 6 #622).

5. Referring to claim 14, an ESD protection device with complementary dual drain implant comprising: a) an N-well, (Figure 6 #612), implanted in a P-substrate, (Figure 6 #21); b) an N+ diffusion, (Figure 6 #624 & 620), implanted on top of said N-well, (Figure 6 #612), such that said N+ diffusion, (Figure 6 #624 & 620), extends into said P-substrate, (Figure 6 #21), on both sides of said N-well, (Figure 6 #612); c) where said N+ diffusion, (Figure 6 #624 & 620), is shared by the drains of two adjacent NMOS transistors, (Figure 6 #626 & 618); d) a pad, (Figure 6 #38), coupled conductively to said N+ diffusion, (Figure 6 #624 & 620), between said drains;

and e) a P-ESD implant interposed between said N+ diffusion, (Figure 6 #624 & 620), and said N-well, (Figure 6 #612), such that said P-ESD implant, (Figure 6 #622), is embedded within said N+ diffusion, (Figure 6 #624 & 620), and said N-well, (Figure 6 #612), where the P-ESD implant, (Figure 6 #622), dosage is chosen in such a way as to counter dope, (p type is the opposite of n type, hence counter doped), said N-well, (Figure 6 #612).

6. Referring to claim 16, an ESD protection device, wherein where said P-ESD implant, (Figure 6 #622), lowers the avalanche voltage of a transistor by reducing the breakdown voltage, (All of the elements of the device as claimed are present in the referenced Figure 6, hence the device would function the same as claimed and Col. 4 Lines 50-60), of the drain- P-substrate junction, (Figure 6 #21).

7. Referring to claim 20, an ESD protection device, wherein said P-ESD implant, (Figure 6 #622), is interposed between said N+ diffusion, (Figure 6 #624 & 620), and said N-well, (Figure 6 #612), such that said N-well, (Figure 6 #612), is electrically coupled to said N+ diffusion, (Figure 6 #624 & 620).

Allowable Subject Matter

8. Claims 2-3, 15, 18, & 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
4/21/05